

(12) United States Patent Agrawal et al.

(10) Patent No.:

US 6,348,813 B1

(45) Date of Patent:

Feb. 19, 2002

(54) SCALABLE ARCHITECTURE FOR HIGH DENSITY CPLD'S HAVING TWO-LEVEL HIERARCHY OF ROUTING RESOURCES

(75) Inventors: Om P. Agrawal, Los Altos, CA (US);
Claudia A. Stanley, Austin, TX (US);
Xlaojie (Warren) He, Austin, TX (US);
Larry R. Metzger, Austin, TX (US);
Robert A. Simon, Colorado Springs,
CO (US); Kerry A. Ilgenstein, Austin,

TX (US)

(73) Assignee: Lattice Semiconductor Corporation, Hillsboro, OR (US)

(*) Notice: Subject to any disclaimer, the term of this patent is extended or adjusted under 35

U.S.C. 154(b) by 0 days.

(21) Appl. No.: 09/721,153

(22) Filed: Nov. 22, 2000

Related U.S. Application Data

(62) Division of application No. 09/326,940, filed on Jun. 6, 1999, now Pat. No. 6,184,713.

(56) References Cited

U.S. PATENT DOCUMENTS

6,097,212 A * 8/2000 Agrawal et al. 326/41

6,150,841 A * 11/2000 Agrawal et al. 326/41

* cited by examiner

Primary Examiner—Michael Tokar Assistant Examiner—Vibol Tan (74) Attorney, Agent, or Firm—Fliesler, Dubb, Meyer & Lovejoy LLP; Gideon Gimlan

(57) ABSTRACT

An improved, scalable CPLD device has a two-tiered hierarchical switch construct comprised of a Global Switch Matrix (GSM) and an even number of Segment Switch Matrices (SSM's). An even number of Super Logic Blocks (SLB's) are coupled to each SSM. Each SSM and its SLB's define a segment that couples to the GSM. Each SLB has a relatively large number of inputs (at least 80) and can generate product term signals (PT's) that are products of independent input terms provided from the SSM to the SLB inputs. Some of the product terms generated within each SLB are dedicated to SLB-local controls. Each SLB has at least 32 macrocells and at least 16 I/O pads which feedback to both to the local SSM and the global GSM. 100% intra-segment connectivity is assured within each segment so that each segment can function as an independent, mini-CPLD. Each SSM has additional lines, dedicated for intersegment (global) communications. The large number of parallel inputs to each SLB ease implementation of 64-bit wide designs. Symmetry within the design of each segment allow for more finely-granulated implementations such as for 32 or 16-bit wide designs.

16 Claims, 16 Drawing Sheets

